JULY 1968

R&D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS

PREPARED BY
PHILCO-FORD CORPORATION
MICROELECTRONICS DIVISION
BLUE BELL, PENNSYLVANIA 19422

PREPARED FOR
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

THIRTEENTH INTERIM REPORT
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UNDER
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THIS REPORT COVERS THE PERIOD
JANUARY 1 TO MARCH 31, 1968

ABSTRACT

A research and development program directed toward the development of technologies for high speed computer subsystems is described.

Increases in the yield of low power, high speed, high density ECL complex logic arrays, made possible by improved multilevel interconnection technologies, are reported. Multi-chip high speed LSI subsystems have been assembled by face-down bonding.

Computer aid has been incorporated into a system for designing and generating photomasks for complex high speed microcircuits. Results are given for a high speed, high density transistor Read Only Memory.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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SECTION I - INTRODUCTION

1.1 PROGRAM OBJECTIVES

The goal of this program is twofold: (1) to establish the technological requirements for achieving very high speed computer systems through fabrication and use of ultrahigh-speed bipolar digital LSI microcircuit arrays; and (2) to develop methods of subsystem assembly which are compatible with high speed system performance.

1.2 SCOPE OF REPORT

This report covers the work performed during the period January 1 to March 31, 1968, on Phase II of the program "R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems". This program is an extension of Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF19(628)-5167) which began in July 1964. The title of this report, Thirteenth Interim Report, is referenced to the beginning of the contract.

1.3 AREAS OF INVESTIGATION

During this period, specific areas of program effort included:

a. A continuing effort to improve fabrication techniques for increasing yield of high speed devices and circuits at the microcircuit level.

b. A continuing effort to develop effective multilevel interconnection structures for high speed arrays. This effort, which was principally directed towards two-level metallization systems, had the primary goals of:

   1. Eliminating or significantly minimizing the array yield losses which are due to via opens.
   2. Developing the techniques necessary for implementing an effective all-aluminum multilevel interconnection system. The vehicles used were the 3-Bit Parity Array and 16 x 16 Read Only Memory Array.

c. Continued cooperation with Lincoln Laboratory personnel to develop computer aided design techniques for the layout of high speed microcircuit arrays. A relatively simple high speed ECL gate (7 transistors and 2 diodes) and a Read Only Memory (256 transistors) were designed for the purpose of proving feasibility and perfecting the design technique. Initial samples of both design structures have been fabricated. Results are described in subsections 2.3, 2.5 and 2.6.

d. Continued experiments with face down bonding techniques for subsystem assembly. Specific efforts were directed toward assembling a 9-Bit Parity Checker subsystem by face down bonding of 3-Bit Parity Arrays onto a silicon interconnection chip.

e. The design and fabrication of a transistor-resistor test chip for the purpose of characterizing and optimizing transistor and resistor designs for future array designs. Wafers of these test chips are also being fabricated to provide statistical data on device yield and parameter spreads.

SECTION II - SPECIFIC DEVELOPMENTS DURING REPORTING PERIOD

2.1 SUMMARY

During this interim, continued evaluations of the high yield microcircuit process described in the Twelfth Interim Report have indicated that the process continues to maintain microcircuit yields at the >90% level on a consistent basis. Transistor yields as high as 98.8% have been measured and also calculated from statistical analysis of yields of completed arrays.

Newly instituted improvements in multilevel interconnection processing have resulted in substantial increases in the yield of arrays having two levels of interconnect metallization. The yield of 3-Bit Parity Arrays (40 transistors, 18 resistors, 31 interconnect vias) has been increased by as much as a factor of five. The improved processing has also enabled the successful fabrication of functional 256-bit Read Only Memory Arrays which contain 256 transistors and 256 vias.

It has been demonstrated that computer aided drafting (CAD) techniques can be implemented to substantially reduce the layout design time of high speed, small geometry microcircuits and microcircuit arrays. A 16-component ECL gate and a 256-component two-level array, both designed using CAD techniques, were successfully fabricated and evaluated.

The first functional high speed, 9-Bit Parity Checker subsystems to be assembled by face down bonding techniques were completed during this period.

A small geometry resistor-transistor test chip intended for characterizing and optimizing transistor and resistor designs for future arrays was designed and fabricated. Samples were delivered to Lincoln Laboratory for evaluation.

2.2 ARRAY FABRICATION

Continued implementation of the high yield microcircuit process described in the Twelfth Interim Report has maintained transistor yields above the 90% level. Several key improvements in multilevel interconnection processing, however, have increased the yields of 3-Bit Parity Arrays with two levels of interconnect metallization by as much as a factor of 5. These techniques have also made possible the successful fabrication of the more complex Read Only Memory Arrays which contain 256 transistors and are also interconnected by two levels of metallization. These processing techniques are now being applied to arrays having three levels of metallization. Initial test results will soon be available.

The specific process improvements referred to immediately above include the return to use of aluminum as the microcircuit level interconnection metal. During the preceding interim, we found it necessary to use a bimetal film for the first level of metallization to minimize the contact resistance between the first and second levels of interconnects (through small-area vias) in two-level arrays. During this interim, optimization of via etching cycles and aluminum evaporation techniques have permitted the implementation of an all-aluminum system with no apparent increase in interlevel contact resistance (also referred to as "via resistance"). We believe the return to all-aluminum metallization has been mainly responsible for the stated yield improvements of two-level arrays. Analyses have suggested that the improvement in yield was strongly related to a tendency on the part of arrays with all-aluminum metallization to better preserve the quality (through the multilevel fabrication process) of emitter-base diodes than is the case in arrays which have the bimetal type of first-level metallization.

A significant factor which still occasionally affects microcircuit level yields is "buried layer washout". "Buried layer washout" refers to the distortion and, at times obliteration, of pre-epitaxy diffused patterns which occur during epitaxial layer growth.

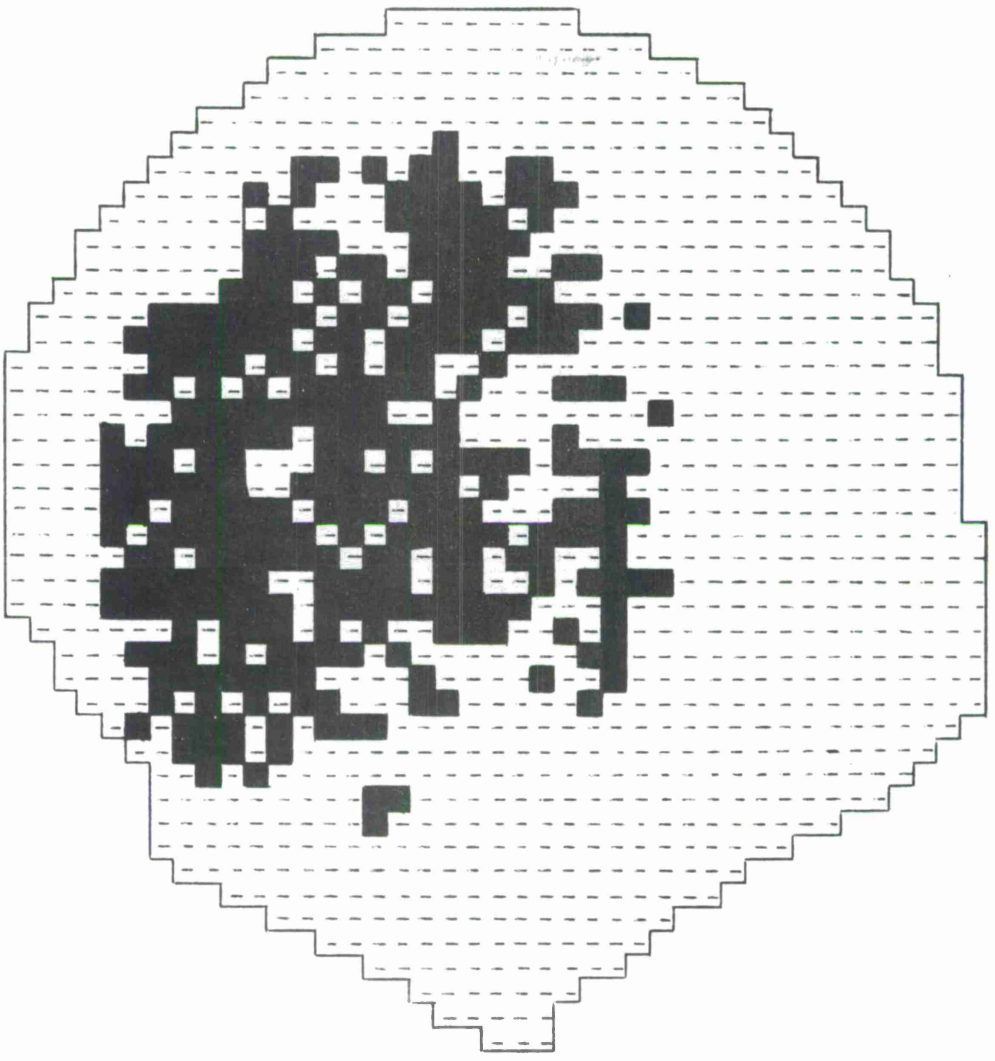
This phenomenon makes difficult the proper location of post-epitaxy device and isolation regions and, in the worst cases, has resulted in device-to-isolation shorts and poor isolation. Techniques are being investigated to minimize the washout phenomenon. One technique being investigated involves increasing the off-orientation angle on the ⟨111⟩ substrate wafers being used from the presently employed 1 to 2° to greater than 3°, with the angle directed toward ⟨110⟩ orientation. Initial results are promising. More detailed information will be obtained during the next interim.

2.3 HIGH SPEED ARRAYS

2.3.1 Two-Level Arrays

2.3.1.1 3-Bit Parity Arrays

The lot of three 3-Bit Parity Array wafers which was fabricated during this period yielded more than 800 functional arrays at die sort. Overall array yields ranged from 10.7% to 31.6%; overall transistor yields calculated from array yields ranged from 94.6% to 97.1%. In the high yield section of one wafer, #17c, which contained 308 functional arrays, array yield was 63.1% and the calculated transistor yield was 98.8%. The die sort map of this wafer is shown in Figure 1. Based on the data given here and die sort maps similar to and including those in Figures 1 and 2, we believe



Total number of functional arrays ---- 314

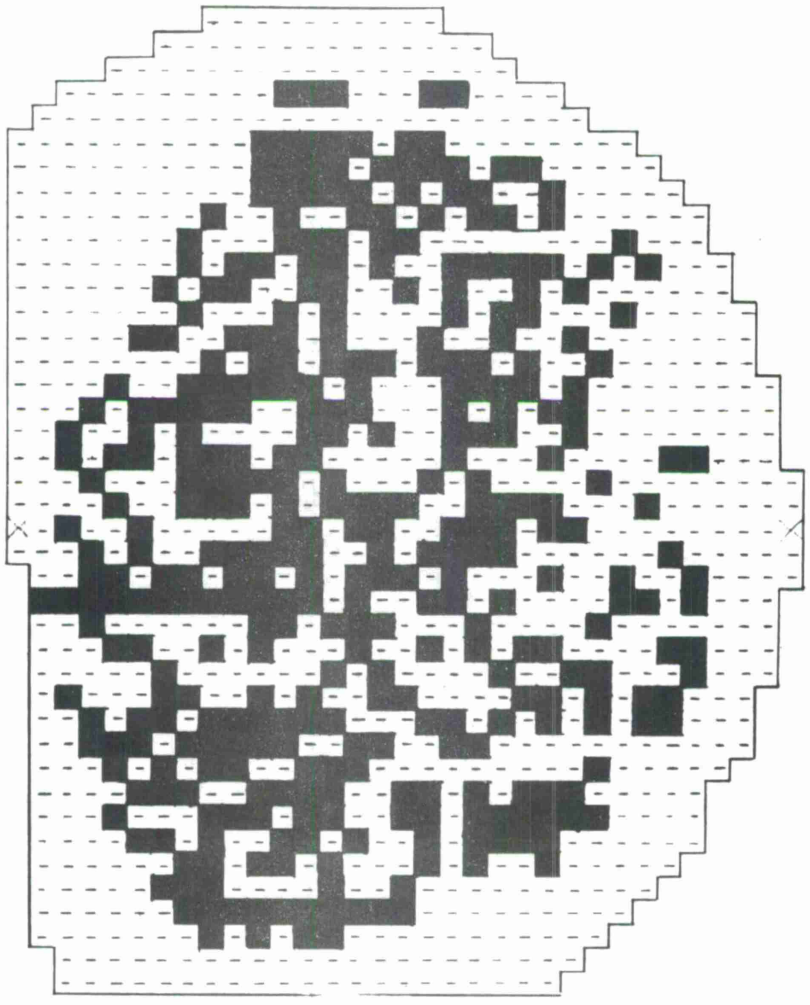
Overall array yield ---------- 24.8%

Array yield in center of wafer ------- 63.1%

Overall calculated transistor yield -- 96.6%

Transistor yield in center of wafer -- 98.8%

Figure 1. Wafer map showing locations of functional 3-Bit Parity Arrays on Wafer #17c.



Total number of functional arrays ---- 363

Overall array yield ---------- 31.6%

Overall calculated transistor yield -- 97.1%

Figure 2. Wafer map showing locations of functional 3-Bit Parity Arrays on Wafer #14d.

our present two-level array process is capable of producing arrays more than four times as complex as the 3-Bit Parity Array, which contains 8 gates and 58 components (40 transistors).

We have no plans to fabricate additional 3-Bit Parity Arrays. The functional chips from the last lot of wafers have been and will be employed for a number of purposes, including:

1. Life test evaluations of two-level arrays fabricated with all-aluminum metallization;
2. Subsystem assembly experiments in which a 9-Bit Parity Checker subsystem is assembled by the face-down bonding of 3-Bit Parity Array chips;
3. Computer aided test and analysis experiments at Lincoln Laboratory.

Sample devices will also be characterized for propagation delay time.

2.3.1.2 Read Only Memory Arrays

A Read Only Memory (ROM) Array chip was designed and first samples were fabricated during this interim. This memory chip, which is capable of storing 16 words at 16 bits per word, is an array of 256 transistors, interconnected in the emitter follower mode by two levels of metallization. Following are some significant features of the ROM chip.

1. The array layout was designed using the computer aided drafting (CAD) techniques described in subsection 2.6. This effort demonstrated the unique capability of computer aid to rapidly and accurately effect layout design of repetitious microcircuit features such as the 16 x 16 transistor matrix of the ROM chip. Figure 3 shows a complete ROM chip. Figure 4 illustrates schematically the ROM chip.

2. The entire active area of the array chip occupies only 256 $mils^2$ (1 mil^2 per transistor, including interconnections). The transistors are 0.1-mil geometry devices, with emitter and base contact cuts which are 0.1 x 0.3 mils and with a base area of 0.05 $mils^2$.

3. The ROM Array was designed to be programmable in chip or package form through selective fusing. Narrow (0.1 mil) emitter metallization fingers were designed to act as fuses which could be electrically "burned open" by electromigration effects induced by passage of high current densities through the narrow aluminum fingers. Metal contacts to the base contact stripes were designed to pass similar currents

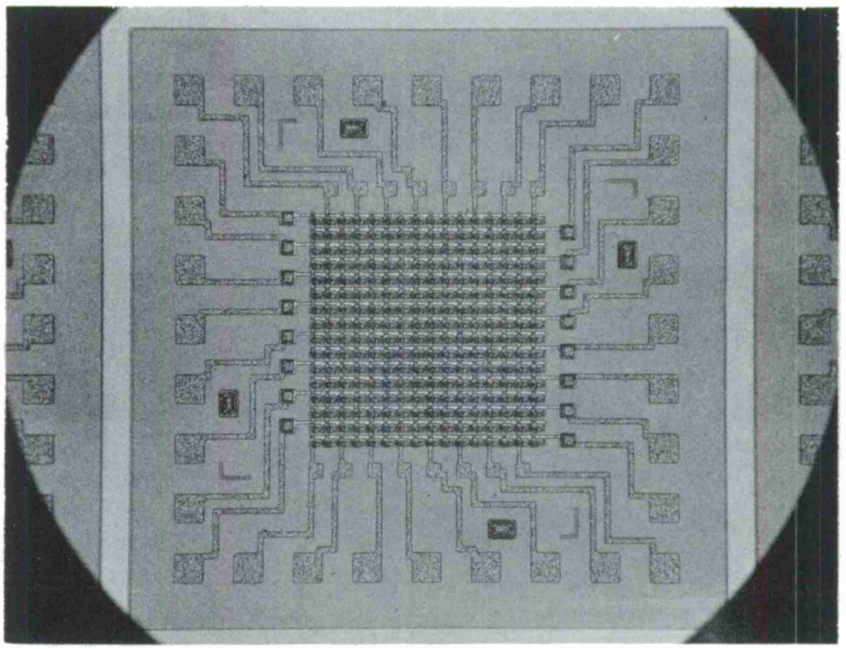


Figure 3. Photomicrograph of 256-Bit Read Only Memory chip.

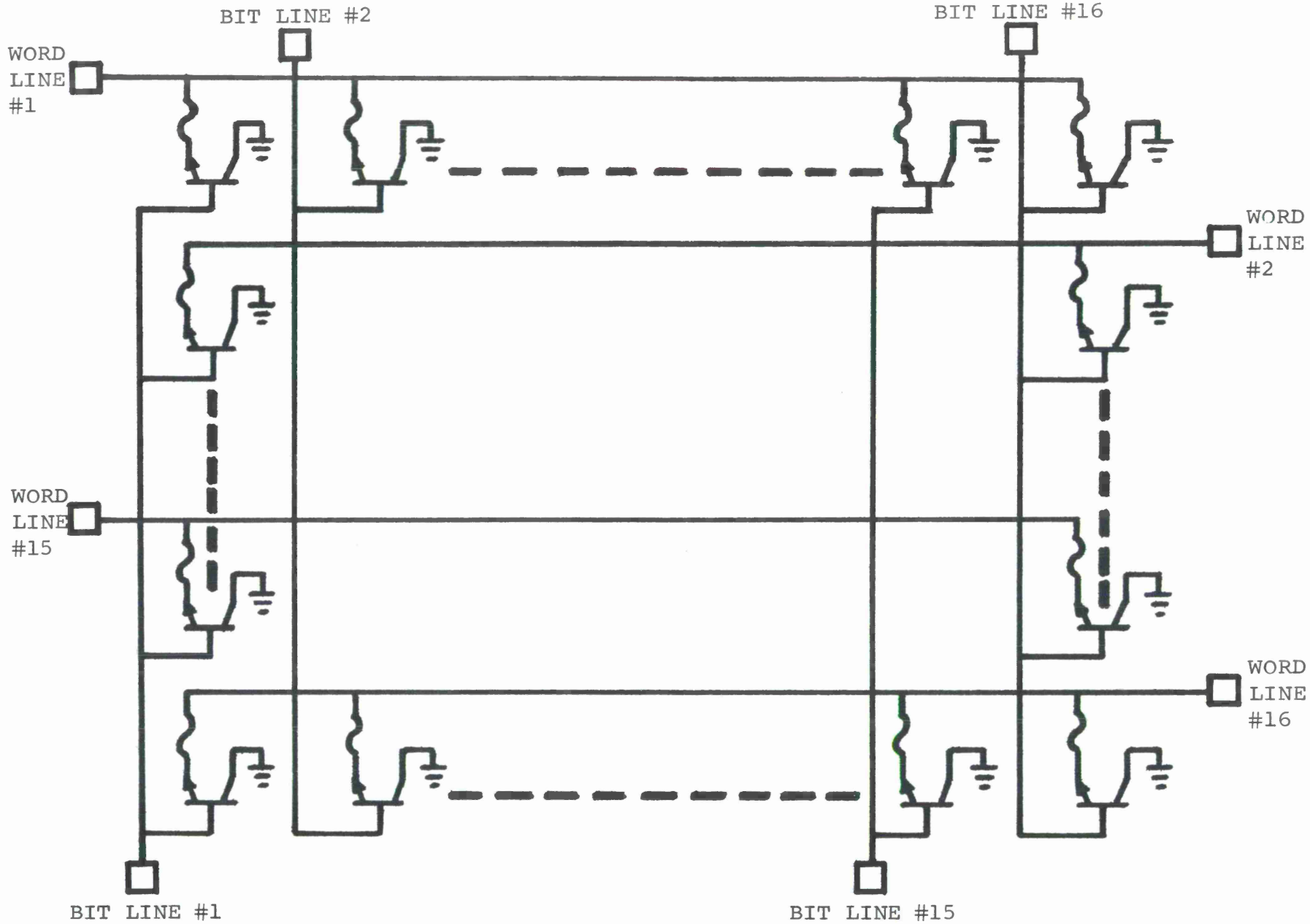


Figure 4. Schematic diagram of Read Only Memory Array.

without being affected by electromigration. Figure 5 illustrates the transistor geometries including the fuses.

4. Interconnection of the ROM requires two levels of metallization and 1 insulator via per transistor; vias are 0.2 x 0.2 mil. The ROM chip, because it contains 256 vias, has been an excellent vehicle for characterizing the improved process for photoengraving of vias in terms of its effectiveness to produce large numbers of small area, low resistance vias.

Die sort evaluations of the first two ROM Array wafers to be produced indicated a yield of four perfect ROM Arrays, with a substantial number of the arrays containing but one or two defective transistors. No via problems were encountered in these arrays. The predominant failure mode encountered was metallization shorts across the narrow (0.1 mil) emitter-base spacing. It is believed that this will be remedied on future devices by optimizing the photoengraving process which is used for delineating the first-level metal.

Sample ROM Arrays from the first two wafers will be packaged and used for fuse-programming experiments. Eight additional wafers of ROM Arrays are in process.

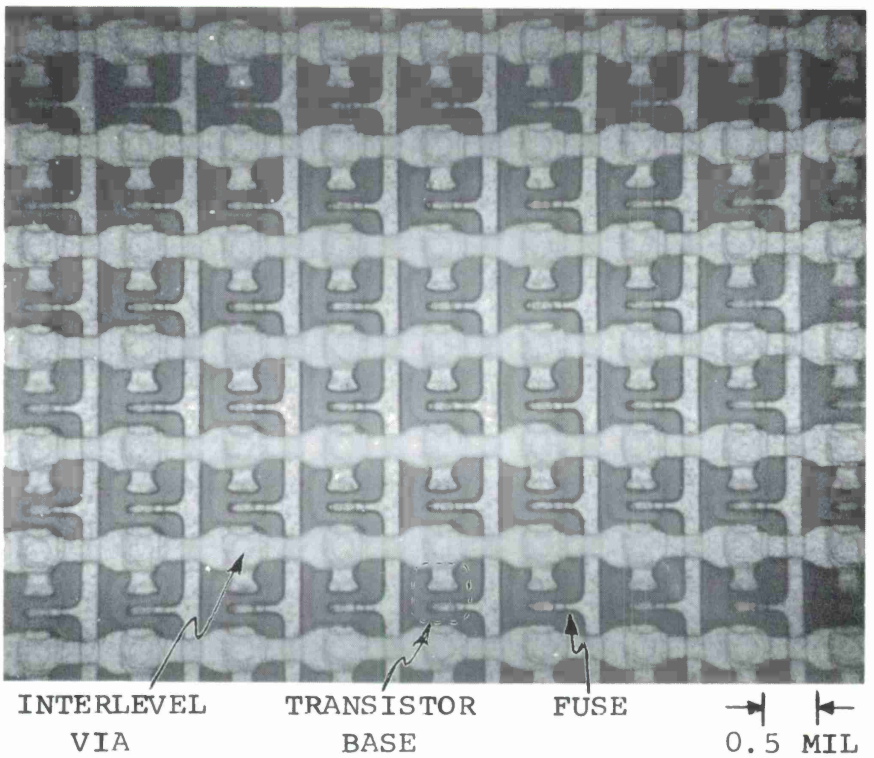


Figure 5. High magnification photomicrograph of 256-Bit Read Only Memory chip.

2.3.2 Three-Level Arrays

Although the main program effort during this interim was focused on the areas enumerated in subsection 1.3, we began to apply to three-level arrays the yield improving technologies which were developed on two-level high speed arrays during this interim. A strong effort will be devoted to three-level arrays during the next interim. The vehicles to be employed in this effort include the Parity Checker Arrays, Functional Multiplier Array and Associative Memory Array, all of which were described in detail in the Twelfth Interim Report. Table I lists some specific information pertaining to these arrays.

2.4 SUBSYSTEM ASSEMBLY BY FACE DOWN BONDING

During this interim several functional 9-Bit Parity Checker subsystems were assembled by face down bonding. The 9-Bit Parity Checker subsystem consists of four 3-Bit Parity Array chips (circuit chips) face down bonded onto a silicon interconnection substrate (wafer-chip). The interconnection substrate is prefabricated with aluminum interconnections and gold interconnect pedestals. Figure 6 illustrates the 9-bit subsystem interconnect chip and the constituent 3-bit circuit chips. Figure 7 shows an assembled subsystem. Face down chip bonding was performed with thermocompression techniques, the heat energy being provided by a constant temperature heat column upon which the assembly

TABLE I

HIGH SPEED 3-LEVEL ARRAYS USED AS PROGRAM VEHICLES

Type of Array	Type of Logic	Component Count		Chip Size ($mils^2$)	No. of Pads	Levels of Interconnects
		Transistors	Resistors			
9-Bit Parity	ECL	160	72	45 x 51	23	3
27-Bit Parity	ECL	520	234	90 x 85	59	3
1 x 1 Functional Multiplier	ECL	120	54	60 x 34	15	3
4 x 4 Associative Memory	RTL	352	424	96 x 75	26	3

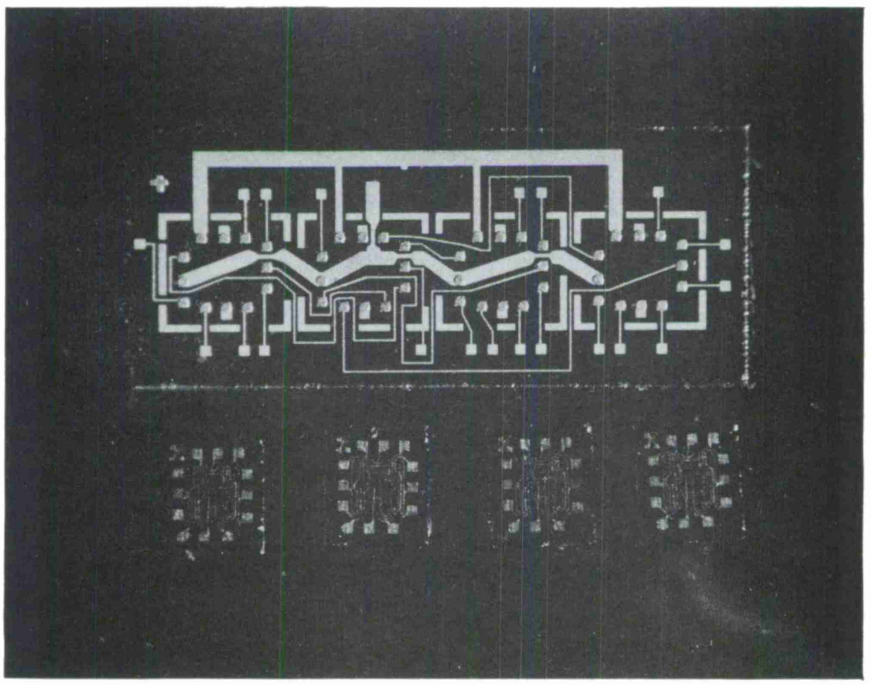


Figure 6. Components (3-bit parity circuit chips and interconnection wafer-chip) for face down bonding assembly of a 9-Bit Parity Subsystem.

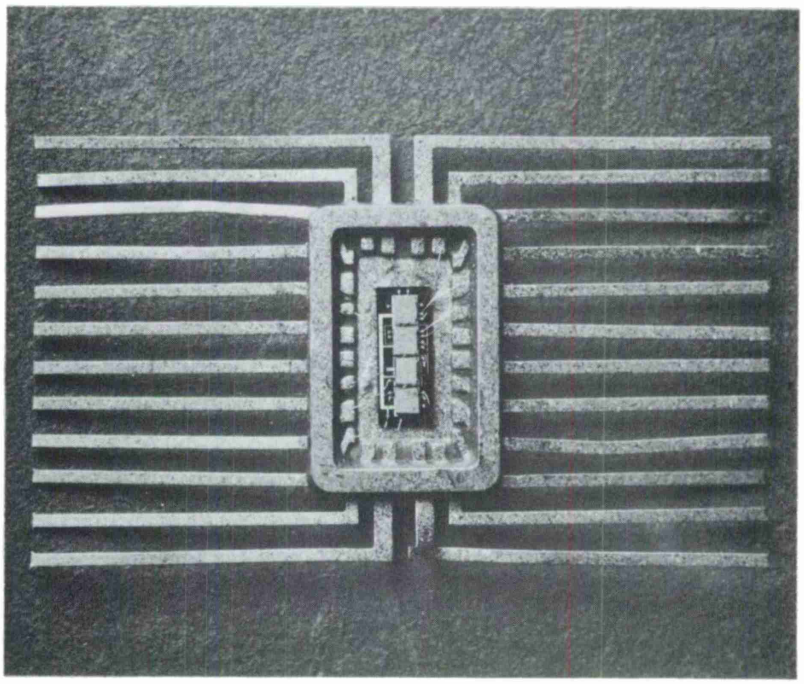


Figure 7. Photograph of a face down bonded 9-Bit Parity Checker subsystem.

is performed. There are 48 gold interconnection pedestals in the 9-Bit Parity Checker subsystem. The pedestals are 2.0 mils in diameter and 9 to 10 microns high.

Experiments are underway to examine the high speed performance and the heat dissipation characteristics of the 9-Bit Parity Checker subsystems. Propagation delay on the subsystems assembled by face down bonding will be compared with propagation delay measured on a 9-Bit Parity Checker assembled using separately packaged 3-Bit Parity Arrays. Preliminary thermal plotting data indicate that the highest chip temperature (room temperature ambient) in an operating 9-bit subsystem dissipating a total of 230 mW ($\approx$ 57 mW per 3-bit chip) is 50 °C.

2.5 HIGH SPEED MICROCIRCUITS

During this interim a new 0.1-mil geometry high speed ECL microcircuit gate (designated SMX12) was designed as part of an experiment to evaluate computer aided drafting as a method for reducing the layout design time for high speed microcircuits and microcircuit arrays. The SMX12 contains seven transistors, two diodes and seven resistors. Figure 8 is a photomicrograph of an SMX12.

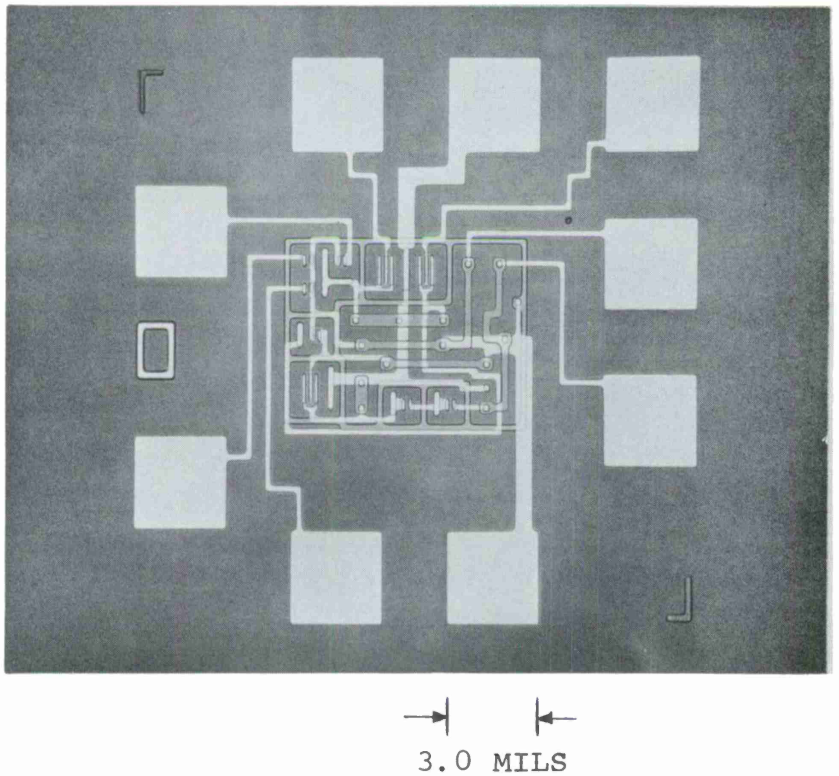


Figure 8. Photomicrograph of SMX12 high speed 0.1-mil geometry ECL gate.

From the circuit design aspect, the SMX12 differs from previously studied ECL gates in that it contains a built-in reference voltage network. Evaluations of this reference network will help in the design of future ECL arrays wherein inclusion of reference voltage networks will be valuable in reducing interconnection complexities by reducing the number of buss lines from three to two. Also, only a single power supply is required.

Functional devices were obtained from the first wafer of SMX12 gates. A shipment of five devices was made to Lincoln Laboratory. Propagation delay measurements will be available soon.

Preliminary die sort data obtained on wafers that were subsequently fabricated suggest that the die sort yields will be excellent. A yield of 50% was obtained on one wafer on which die sort testing was completed. This evidence indicates that high speed, high yield microcircuit layout designs can be generated using computer aided drafting techniques. Higher yields can be expected on future designs when certain refinements in the computer program and design rules are made. As an example, a major yield loss factor has been aluminum-to-aluminum shorts caused by non-optimum design of the metallization masks, partly due to design compromises necessitated by the present computer program.

2.6 COMPUTER AIDED DRAFTING (CAD)

In the conventional mask making processes, much of the time necessary to produce the photomasks for a specific microcircuit or microcircuit array is the time used in layout design and in generation of artwork. It is believed that with the computer aid the time required for the operations can be reduced substantially. This reduction in mask generation time would significantly reduce turn-around time and very probably lower the cost. It is also believed that computer aid will result in a lower incidence of artwork errors, especially on complex masks containing repetitive patterns.

In a cooperative effort between Lincoln Laboratory and Philco-Ford, photomask layouts for a single ECL gate (Figure 8) and a complex ROM array (Figure 3) were designed using CAD techniques. This design effort was followed by generation of working masks and fabrication of the design structures. The purpose of this effort was to determine how the use of CAD techniques in the design of small geometry, high frequency microcircuits and arrays can affect turn-around time, cost and yield. The following sequence of steps was used to produce the indicated mask sets.

1. A designer generated the equivalent of a composite layout drawing and separate photomask drawings. This step

involved use of a Sylvania grid tablet, a computer which was programmed with appropriate design rules, and a CRT display. The coordinate data for patterns of these layouts were stored by the computer. On prescribed commands the layouts were punched out in code on tape.

2. The tape was fed into a commercial pattern generator which generated 10X reticles for each photomask drawing.
3. Each reticle was then processed into working photomasks using conventional microstepping techniques.

From the results of the CAD effort described above, it is concluded that small geometry (0.1 mil) microcircuits and arrays can be designed using CAD techniques and commercial pattern generation equipment. It was found that a substantial improvement in turn-around time is realized. For example, the total time required to produce completed photomasks for the SMX12 ECL gate was reduced by a factor of three to five compared to the conventional methods of photomask design and processing. Concerning layout design accuracies, no errors were found in either the simple SMX12 mask set or in the complex ROM mask set. Concerning yield, even though program limitations restricted optimum design in some parts of the SMX12, microcircuit yields at die sort ran as high as 50% on the first wafer lot that was processed. In

addition, functional ROM arrays were obtained on the first lot of wafers to be processed. Concerning cost, there is difficulty in assessing at this time the level of improvement that might be realized if all operations were carried out on a commercial basis. However, within the limits of this specific CAD evaluation, which used a computer and a developed graphics capability of Lincoln Laboratory, there definitely was a reduction in overall cost to produce the SMX12 and the ROM.

2.7 PROPOSED FOLLOW-ON PROGRAM

A new follow-on program is being negotiated with Lincoln Laboratory. The proposal for the program is in the final stages of preparation.

A major task of the proposed follow-on program would be to develop a set of high speed microcircuit array chips to form the central processor of an experimental computer. A new ECL gate design would be required. In preparation for this new gate design, we have completed a panic mask set consisting of four different 0.1-mil geometry transistors and a variety of resistor configurations (ranging from 0.2 mil to 0.5 mil) which span the anticipated design spectrum, and have fabricated wafers of devices. The test chip also contains sheet resistance test structures for transistor base regions and for resistors. Figure 9 is a photomicrograph of the test chip, designated SPX1.

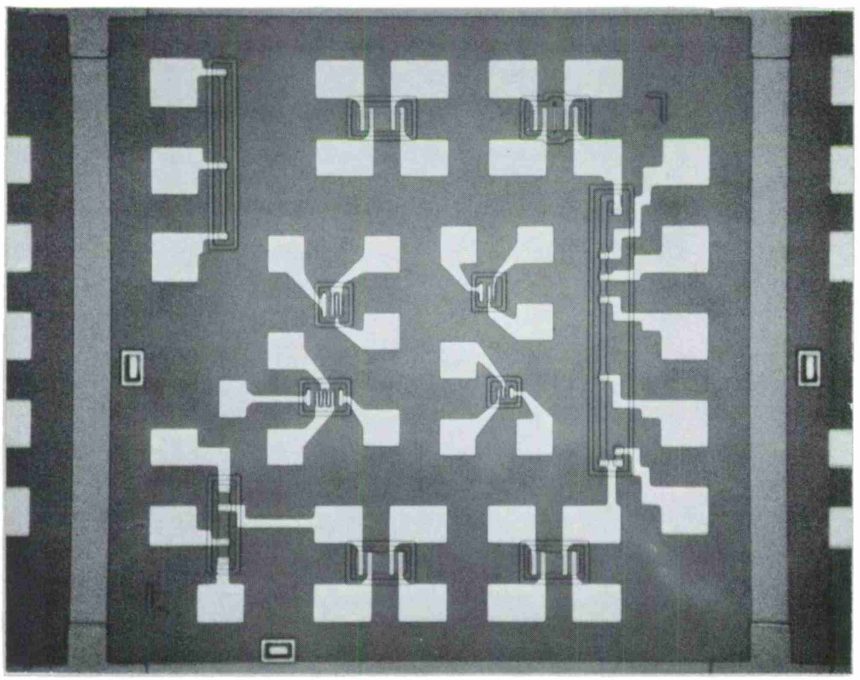


Figure 9. Photomicrograph of high speed test chip containing 0.1-mil geometry transistors, small geometry resistors, and test patterns for device-diffusion sheet resistance.

Sixty packaged SPX1 chips were delivered to Lincoln Laboratory. The transistors in these first chips were not isolated. A second group of wafers containing isolated transistors is being fabricated.

Complete evaluations of these devices should provide a firm base for the layout design of the central processor chips.

2.8 DELIVERIES

During this interim the device deliveries to Lincoln Laboratory included five SMX12 gates and 60 packaged SPX1 test chips.

SECTION III - FUTURE PLANS

The program plan for the remaining three months interim of this contract is to concentrate heavily on arrays having three levels of interconnect metallization. This effort will include implementation of the improved two-level interconnection fabrication methods (see paragraph 2.3.1) to the various three-level arrays which have been designed. These include the 9-Bit and 27-Bit Parity Arrays, the Functional Multiplier Array and the Associative Memory Arrays.

Other program tasks planned for the final interim include:

1. Continued evaluation of methods for improving yields.
2. Continued fabrication and evaluation of ROM arrays.

   Specific goals will be to:

   a. Improve yield

   b. Investigate the reliability and reproducibility of programming the ROM by means of electronic fusing.
3. Evaluate the performance of the SMX12 ECL gate.
4. Complete and evaluate the SMX9 ECL gate.
5. Fabricate and evaluate SPX1 test chips containing isolated transistors.

6. Evaluate the thermal dissipation properties and the performance characteristics of 9-Bit Parity Checker subsystem assembled by face down bonding techniques.

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14. KEY WORDS

microcircuit arrays
large scale integration (LSI)
face down bonding
multilevel interconnection
computer aided drafting (CAD)